IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

EMC CORPORATION, EMC INTERNATIONAL COMPANY, and EMC INFORMATION SYSTEMS INTERNATIONAL,	)	
Plaintiffs,	)	C.A. No. 13-1985 (RGA)
v.	)	
PURE STORAGE, INC.,	)	
Defendant.	)	

[CORRECTED] JOINT CLAIM CONSTRUCTION CHART

Pursuant to Paragraph 9 of the Court's February 21, 2014 Scheduling Order (D.I. 16), the parties hereby submit the [Corrected] Joint Claim Construction Chart attached as Exhibit 1. The Chart contains the parties' respective proposed constructions for the disputed claim terms and phrases from U.S. Patent Nos. 6,904,556, 6,915,475, 7,434,015, 7,373,464, and 8,375,187, as well as citations to the relevant portions of the intrinsic record[1] relied upon by the parties. The parties reserve the right to rely upon the intrinsic evidence cited by the other. The parties further reserve the right to rely upon other portions of the intrinsic record in rebuttal.

The parties agree on the following constructions:

1. '475 patent, claim 1: "predetermined" means "calculated by a source external to the storage system."

2. '475 patent, claim 1: "multiple-block error detecting code" means "an error detecting code calculated from each of the data values in the plurality of blocks of data."

[1] In the attached Chart, citations to patents are provided in the format [column number]:[starting line number]-[ending line number]. For example, "1:1-2" refers to column 1, lines 1-2.

3. '475 patent, claim 1: "individual error detecting code" means "an error detecting code calculated from each of the data values in one of the blocks in the plurality of blocks of data."

4. '475 patent, claim 14: "the transmitted blocks of data" refers to the blocks of data transmitted by the plurality of hosts.

5. '475 patent, claim 14: "the error detection information" refers to the error detection information that was applied and stored by the first data block integrity unit.

6. '475 patent, claim 14: "the stored blocks of data" refers to the blocks of data that were transmitted by the plurality of hosts.

7. '464 patent, claims 1, 19, 32: "a data segments" contains a typo and means "a data segment."

8. '464 patent, claim 19, and '015 patent, claim 15: "segment redundancy check engine" means "module for checking with low latency memory whether segments are already stored."

9. '015 patent, claims 1, 15, 16: "space-efficient" means "taking up less memory space than the stored data segments."

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EXHIBIT 1

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
1.	"memory region"	'556 patent - claims 1, 6, 10, 15	A subset of memory on a memory board that can be accessed simultaneously with other memory regions	U.S. Patent No. 6,904,556 (Exhibit A) at 1:49-62, 3:25-33, 4:10-15, 4:20-36, 7:26-9:51, 13:42-14:24; Figs. 3, 4; claims 1, 6, 10, 15. U.S. Patent No. 6,636,933 (incorporated in its entirety in the '556 patent at 7:26-31) (Exhibit F) at 11:7-12:31, 12:43-45, 14:12-18:8, 18:41-56, 20:58-21:2; Figs. 8A, 9A, 9B, 9C, 10; claim 5. U.S. Patent No. 6,804,794 (incorporated in its entirety in the '556 patent at 9:45-51 [by incorrect number, *see* '556 File History, Amendment, Oct. 29, 2004 (Exhibit H) at	a portion of a memory board that is separately byte addressable by the cache memory system	'556 patent (Exhibit A) at 1:59-62, 7:55-8:23, 9:39-43, 14:44-45; Fig. 4; Claim 1; '933 patent (Exhibit F) at 12:46-47, 14:14-17; '794 patent (Exhibit G) at 7:36-42, 1:49-2:33. See citations regarding "memory system," "memory boards," and "memory segments," incorporated by reference.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				EMC-PS0000358, substituting incorrect patent number for Application No. 09/796,259]) (Exhibit G) at 1:25-2:63, 3:49-54, 7:37-9:22, 12:56-13:7; Figs. 3, 4. '556 file history excerpts (Exhibit H) at July 29, 2004 Office Action (EMC-PS0000267-278), October 29, 2004 Response to Office Action (EMC-PS0000358-379), February 10, 2005 Notice of Allowance (EMC-PS0000383). U.S. Patent No. 5,218,691 (Exhibit L) at 4:38-58, 26:59-27:56; Figs. 3A, 3B.		
2.	"base memory address"	'556 patent - claims 1, 6, 10, 15	An address used as a reference point to which a relative	'556 patent (Exhibit A) at 3:29-33, 4:20-36, 8:4-7, 13:42-	lowest physical memory address of a memory segment	'556 patent (Exhibit A) at 3:29-33, 8:4-7, 14:48-52; Claim 1;

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
			address may be added to determine the address of the storage location to be accessed	14:24; claims 1, 6, 10, 15. '556 file history excerpts (Exhibit H) at July 29, 2004 Office Action (EMC-PS0000267-278), October 29, 2004 Response to Office Action (EMC-PS0000358-379), February 10, 2005 Notice of Allowance (EMC-PS0000383).		'794 patent (Exhibit G) at 8:23-34, 2:6-14, see '556 file history excerpts (Exhibit H) at EMC-PS0000359.
3.	"memory board"	'556 patent - claims 1, 5, 6, 10, 14, 15	Plain and ordinary meaning	'556 patent (Exhibit A) at 2:39-42, 4:10-15, 4:20-36, 7:35-9:51, 13:42-14:24; Figs. 3, 4; claims 1, 5, 6, 10, 14, 15. '556 file history excerpts (Exhibit H) at July 29, 2004 Office Action (EMC-PS0000267-278), October 29, 2004 Response to Office	cache memory board(s)	'556 patent (Exhibit A) at 1:52-56, 2:39-41; '933 patent (Exhibit F) at 12:40-46; 14:12-24. See citations regarding "memory system," incorporated by reference.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				Action (EMC-PS0000358-379), February 10, 2005 Notice of Allowance (EMC-PS0000383). '691 patent (Exhibit L). Holland, M., et al.: "Fast, On-Line Failure Recovery in Redundant Disk Arrays" (Exhibit M) at 422-24.		
4.	"memory system"	'556 patent - claims 1, 2, 5-8, 10, 15	No construction needed; this term appears only in the preamble, which is not limiting	'556 patent (Exhibit A) at 1:5-9, 2:32-39, 4:20-36, 13:42-14:24; Abstract; claims 1, 2, 5-8, 10, 15. '556 file history excerpts (Exhibit H) at July 29, 2004 Office Action (EMC-PS0000267-278), October 29, 2004 Response to Office Action (EMC-	cache memory system	'556 patent (Exhibit A) at 1:52-56, 2:34-41, 3:7-9, 3:50-61, 4:7-15, 6:41-51, 6:56-7:2, 7:17-24, 7:31-36, 8:64-9:2; Figs. 2, 3, 4; '933 patent (Exhibit F) at Figs. 1, 2, 3, 4, 1:38-48; '794 patent (Exhibit G) at 3:14-17, 7:36-

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				PS0000358-379), February 10, 2005 Notice of Allowance (EMC-PS0000383). '691 patent (Exhibit L). Holland, M., et al. (Exhibit M) at 422-24.		42.
5.	"memory segments"	'556 patent - claims 1, 5-7, 10, 14-16	Plain and ordinary meaning	'556 patent (Exhibit A) at 2:42-3:6, 3:25-33, 4:13-36, 7:55-11:6, 13:42-14:24; Figs. 4, 5; claims 1, 5-7, 10, 14-16. '556 file history excerpts (Exhibit H) at July 29, 2004 Office Action (EMC-PS0000267-278), October 29, 2004 Response to Office Action (EMC-PS0000358-379), February 10, 2005 Notice of Allowance	a predetermined-size portion of cache memory that is separately byte addressable by the cache memory system	'556 patent (Exhibit A) at 3:29-33, 7:66-8:4, 8:4-7, 8:23-28, 14:48-52; Claim 1; '933 patent (Exhibit F) at 14:39-49; '794 patent (Exhibit G) at 8:23-34. See citations regarding "memory system," and "memory boards," incorporated by reference.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				(EMC-PS0000383). Holland, M., et al. (Exhibit M) at 422-24.		
6.	"logical exclusive-or" / "logically exclusive-or-ing"	'556 patent - claims 1, 6, 8, 10, 15, 17	"logical exclusive-or": A logic operation that outputs 'true' whenever an odd number of inputs are 'true' and otherwise outputs 'false'. For example, if three inputs are all '1', the output is '1'. If three inputs are '1' '0' '1', the output is '0' "logically exclusive-or-ing": Performing a logical exclusive-or operation	'556 patent at 2:59-3:6, 3:34-49, 4:20-36, 10:60-11:6, 11:17-12:19, 12:47-13:8, 13:42-14:24; claims 1, 6, 8, 10, 15, 17. '556 file history excerpts (Exhibit H) at July 29, 2004 Office Action (EMC-PS0000267-278), October 29, 2004 Response to Office Action (EMC-PS0000358-379), February 10, 2005 Notice of Allowance (EMC-PS0000383). Holland, M., et al. (Exhibit M) at 422-24.	combining via the logical bit-wise boolean XOR operation	'556 patent (Exhibit A) at 2:61-63, 2:65-3:6, 3:39-49, 10:60-11:6.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				U.S. Patent No. 5,954,822 (Exhibit N) at 4:3-45, 15:3-20.		
7.	"block(s) of data"	'475 patent - claims 1, 2, 14	Plain and ordinary meaning	U.S. Patent No. 6,915,475 (Exhibit B) at 1:19-26, 1:46-47, 2:16-58, 3:30-31, 3:36-39, 3:42-45, 3:58-64, 4:8-35, 4:41-43, 4:52-57, 5:1-24, 5:31-47, 5:55-64, 5:67-6:3, 6:7-13, 6:19-35, 6:45-64; Figs. 2, 4, 5, 7; claims 1, 2, 5, 7, 8, 9, 12, 14.	fixed-size unit(s) of data	'475 patent (Exhibit B) at 1:44-47, 2:62-65, 2:43-45, 5:1-2, 5:19-24, 5:41-47, 5:60-62, 6:18-25, 6:21-30, 6:48-59; Symmetrix 3000 and 5000 Enterprise Storage Systems Product Description Guide, EMC Product Description Guide L702.4, Feb. 1999 (incorporated by reference in the '475 patent at 1:36-42) (Exhibit I) at 13.
8.	"storing"	'475 patent - claims 1, 2, 14	Plain and ordinary meaning	'475 patent (Exhibit B) at 4:35-40, 4:44-47, 4:52-55, 5:24-30, 5:60-64, 6:60-64; Abstract; Figs. 3, 4, 5; claims 1, 2, 8, 9, 14, 16, 17.	writing to disk or other nonvolatile storage device	'475 patent (Exhibit B) at 1:6-8, 1:43-52, 2:7-8, 2:46-48, 3:1-3, 3:42-45, 4:24-28, 5:8-11, 5:24-27, 8:1-3; Claim 8.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
9.	"channel adapter"	'475 patent - claims 14, 15, 17	A module that sends data to or receives data from a channel	'475 patent (Exhibit B) at 3:32-36, 3:65-67, 4:8-21, 4:24-5:7, 5:55-6:13, 6:24-35, 6:48-64; Figs. 3, 4; claims 14, 15, 17.	front-end device interfacing between host(s) and global memory	'475 patent (Exhibit B) at 3:65-4:7, 3:14-21, 4:8-14, 4:24-40, 8:39-41; Figs. 3, 4, and 5; Claim 17; Symmetrix 3000 and 5000 Guide (Exhibit I) at 5, 10, 13, and 14-16.
10.	"storage array adapter"	'475 patent - claims 14, 17	A module that stores data in or retrieves data from a storage array device	'475 patent (Exhibit B) at 3:32-34, 3:37-38, 3:67-4:2, 4:21-23, 5:8-54, 6:36-44, 6:48-64; Abstract; Figs. 3, 5; claims 14, 16, 17.	back-end device interfacing between global memory and disk or other nonvolatile storage device(s)	'475 patent (Exhibit B) at 3:7-8, 3:14-21, 3:65-4:7, 4:35-40, 5:8-16, 5:31-34, 8:39-41; Figs. 3, 4, and 5; Claim 17; Symmetrix 3000 and 5000 Guide (Exhibit I) at 5, 10, 14-16, and 19.
11.	"applying"	'475 patent - claim 14	Attaching to the blocks of data	'475 patent (Exhibit B) at 1:19-25, 1:44-55, 2:41-58, 3:30-31, 3:42-45, 4:25-29, 5:1-7, 5:31-49, 6:24-35, 6:49-59; Figs. 2, 4-7; claims 8, 14.	appending	'475 patent (Exhibit B) at 1:19-25, 5:1-7, 5:39-41, 6:20-32.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
12.	"storage array device"	'475 patent - claim 14	Plain and ordinary meaning	'475 patent (Exhibit B) at 2:6-15, 2:24-26, 2:66-3:21, 3:32-35, 3:38-39, 3:51-58, 3:65-4:2, 6:45, 6:60-64; Fig. 3; claims 1, 8, 14, 16.	disk or other nonvolatile storage device in an array	'475 patent (Exhibit B) at 1:43-52, 2:62-65, 3:1-21, 3:55-58, 4:32-34, 5:8-11, 5:26-34, 5:39-41, 6:16-19, 6:36-39; Fig. 3; Symmetrix 3000 and 5000 Guide (Exhibit I) at 5, 10, 13, 14-16, and 19.
13.	"associated with the transmitted blocks of data"	'475 patent - claim 14	Plain and ordinary meaning	'475 patent (Exhibit B) at 1:9-12, 1:26-30, 1:44-49, 3:58-64, 4:31-40, 6:5-6; 6:60-64; Figs. 3, 4; claims 14-16.	individually calculated from each of the transmitted block(s) of data	'475 patent (Exhibit B) at 2:16-19, 2:20-23, 3:1-12, 3:58-64, 4:24-28, 5:67-6:3, 6:28-35; Figs.2 and 7; Claim 8, Symmetrix 3000 and 5000 Guide (Exhibit I) at 26; Symmetrix 5000 Enterprise Storage Systems, EMC Data Sheet L741.2, Dec. 1998 (incorporated by reference in the '475 patent at 1:36-42) (Exhibit J) at 3.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
14.	"identifier(s)"	'464 patent - claims 1, 3, 5, 13, 19, 21, 32 '015 patent - claims 1, 2, 4, 13, 15, 16	Plain and ordinary meaning	U.S. Patent No. 7,373,464 (Exhibit C) at 2:36-52, 3:19-37, 3:50-54, 3:62-4:2, 5:16-6:17, 7:21-38, 7:58-8:20, 9:60-10:2; Abstract; claims 1, 3-6, 13, 19, 21, 32. U.S. Patent No. 7,434,015 (Exhibit D) at 2:33-49, 3:15-32, 3:45-49, 3:57-60, 5:10-6:9, 7:13-29, 7:49-8:9, 9:41-50; Abstract; claims 1-6, 13, 15, 16.	unique value for an individual data segment	'464 patent (Exhibit C) at Abstract, 3:19-21, 3:29-37, 5:9-13, 6:8-13, 7:21-33, 8:17-20, 10:5-7, 10:26-27, 11:18-20, 12:38-40; Claims 1, 19 and 32. '015 patent (Exhibit D) at 3:15-16, 3:25-32, 5:3-7, 5:67-6:5, 7:19-24, 8:7-9; 9:56-57, 11:7-8, Claims 1, 4 13 and 16.
15.	"low latency memory"	'464 patent - claims 1, 5, 19, 32	A memory or cache that can generally be read more quickly or has better throughput than the large memory that stores the entire segment database	'464 patent (Exhibit C) at 2:28-52, 3:50-4:14, 9:60-10:2; claims 1, 5, 19, 32.	directly addressable cache or buffer memory (such as RAM, DRAM, or NVRAM)	'464 patent (Exhibit C) at Abstract, 1:64-67, 2:62-65, 3:42-49, 3:54-62, 5:49-51, 5:35-44, 6:17-18, 6:20-25, 9:56-59, 10:8-10, 11:21-26, 12:42-44; Claims 1, 19 and 32.
16.	"returning" / "return"	'464 patent - claims 1, 19, 32	Plain and ordinary meaning	'464 patent (Exhibit C) at 2:13-14, 2:17-19, 2:28-52, 3:42-52,	delivering back to the calling routine / deliver back to the	'464 patent (Exhibit C) at Abstract, 7:50-53, 7:58-60 , 8:27-29,

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				7:50-60, 8:21-23, 8:21-44, 9:60-10:2; Figs. 2, 4A, 4B; claims 1, 19, 32.	calling routine	8:40-43, 10:11-13, 11:21-26, 12:45-47; Figs. 4A and 4B; Claims 1, 19 and 32.
17.	"determine" / "determined" / "determining"	'464 patent - claims 1, 19, 32 '015 patent - claims 1, 15, 16	"determine": Decide, either conclusively or inconclusively. "determined": Decided, either conclusively or inconclusively. "determining": Deciding, either conclusively or inconclusively.	'464 patent (Exhibit C) at 2:56-67, 3:42-52, 3:62-4:2, 5:16-17, 5:37-67, 7:39-8:20; Abstract; claims 1, 2, 7, 16-19, 23, 29-32. '015 patent (Exhibit D) at 2:53-63, 3:36-47, 3:57-64, 5:10-11, 5:31-59, 7:30-8:9; Abstract; claims 1, 6-10, 15, 16.	conclusively decide / conclusively decided / conclusively deciding	'464 patent (Exhibit C) at 5:45-67, 7:58-63, 10:14-18, 10:63-11:16, 11:27-31, 12:17-34; Claims 2, 16,17, 18, 20, 29, 30 and 31. '015 patent (Exhibit D) at 5:38-59, 7:49-54; Claims 9, 10.
18.	"receiving a data stream" / "receive an input data stream" / "receive a data stream"	'464 patent - claims 1, 19, 32 '015 patent - claims 1, 15, 16	Plain and ordinary meaning	'464 patent (Exhibit C) at 1:31-39, 1:51-54, 2:11-12, 2:15-16, 2:53-59, 3:1-28, 6:39-49; Abstract; Figs. 1, 3; claims 1, 19, 32. '015 patent (Exhibit D) at 1:30-37, 1:48-55, 2:10-11, 2:14-15, 2:52-56, 2:64-3:23, 6:31-41; Abstract;	acquiring sequential data segments from an external source / acquire sequential data segments from an external source	'464 patent (Exhibit C) at 1:31-36, 3:1-6, 3:6-18, 3:35-37, 4:47-52, 7:21-29, 8:33-39, 8:41-43, 9:52-53; Figs. 1, 2, 4B. '015 patent (Exhibit D) at 1:30-35, 2:64-3:14, 3:31-32, 4:40-46, 7:13-21, 8:22-31, 9:33-35; Fig. 4B.

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				Figs. 1, 3; claims 1, 15, 16.		
19.	"probabilistic summary"	'015 patent - claims 1, 15, 16	A data structure that indicates, with possible uncertainty, whether a data segment is already stored	'015 patent (Exhibit D) at 2:33-49, 3:57-64, 5:38-59, 7:66-8:9, 8:48-58, 9:41-50; claims 1, 6-10, 15, 16.	low latency memory subsystem (such as a Bloom filter), that can conclusively determine that a received data segment has not already been stored	'015 patent (Exhibit D) at Abstract, 3:57-60, 5:38-59, 7:51-60, 7:61-8:3; 8:48-61, 8:62-9:24, 9:15-18, 9:37-40, 9:58-61, 10:56-67, 10:61-67, 12:1-4; Figs. 6A and 6C; Claim 1, 14, 15 and 16.
20.	"cache"	'015 patent - claim 8	Quickly accessible memory	'015 patent (Exhibit D) at 2:33-49, 3:45-57, 3:61-64, 5:10-17, 5:29-37, 5:60-6:11, 6:51-7:12, 7:45-48, 8:10-16, 9:41-50; claim 8.	low latency memory subsystem containing a subset of identifiers that can conclusively determine that a received data segment has already been stored	'015 patent (Exhibit D) at 5:29-37, 5:38-59, 5:60-6:11, 9:37-40, 10:19-20, 10:22-31, 10:34-42; Fig. 4B; Claims 8, 9 and 10.
21.	"relatively high latency memory"	'015 patent, claim 7	Storage that cannot be accessed as quickly as the memory that stores the summary	'015 patent (Exhibit D) at 2:33-49, 3:45-4:9, 5:41-44, 5:57-59, 7:45-48, 8:32-34, 9:41-50; claims 1, 7-10.	"relatively": Indefinite; not capable of construction. "high latency memory": protocol- or network-attached storage that stores the segment database	'015 patent (Exhibit D) at 1:60-63, 3:49-57, 3:64-4:14, 5:41-44, 5:57-59, 6:12-13, 5:29-37; Figs. 1 and 2; Claims 9 and 10; '464 patent (Exhibit C) at Claim 9; *see*

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
					(such as magnetic, optical, or solid state disk) Pure Storage's position is that the appropriate term to construe is "high latency memory" without the qualifier "relatively."	*also* citations for "low latency memory," incorporated by reference.
22.	"a" in the phrase "a triggering event"	'187 patent - claims 1, 5, 9, 12	One or more	U.S. Patent No. 8,375,187 (Exhibit E) at 1:51-58, 2:3-8, 6:26-56, 8:49-51, 9:50-56, 10:26-28, 12:18-34; claims 1, 5, 9, 12.	Construction is not necessary.	
23.	"scheduled"	'187 patent - claims 1, 5, 9, 12	Plain and ordinary meaning	'187 patent (Exhibit E) at 1:39-43, 1:63-67, 5:40-62, 7:40-48, 8:26-30, 9:13-22, 9:61-65, 12:18-34; claims 1, 5, 9, 12.	currently selected by the controller in accordance with a scheduling policy	'187 Patent (Exhibit E) at 5:2-9, 5:58-59, 7:19-25, 8:18-30, 9:50-56, 9:61-65, 9:67-10:2, 10:5-10, 11:28-33, 11:37-40; Figs. 5, 9, 11, 14, 15, 18, 19; '187 patent file history, Office Action

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
						Summary dated February 16, 2011 (Exhibit K) at EMC-PS0002453-EMC-PS0002454. '187 patent file history, Amendment and Response dated July 14, 2011 (Exhibit K) at EMC-PS0002475-EMC-PS0002481, EMC-PS0002468. '187 patent file history, Request for Reconsideration dated June 18, 2012 (Exhibit K) at EMC-PS0002544-EMC-PS0002546.
24.	"buffer memory"	'187 patent - claims 1, 5, 9, 12	Memory for temporary storage of data	'187 patent (Exhibit E) at 2:21-22, 2:30-31, 2:40-43, 2:52-53, 3:31-33, 3:37-42, 4:4-13, 5:9-11, 5:14-16, 5:36-38, 6:20-25, 7:26-28, 12:18-34;	cache in global memory for temporary data retention	'187 patent (Exhibit E) at 3:37-42, 3:55-63, 4:14-19, 5:14-16, 5:20-24, 5:36-38, 6:20-25 , 7:26-28; 7:32-36, 10:2-4, 10:20-23, 11:33-36;

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
				Figs. 2, 5, 9, 14; claims 1, 5, 9, 12.		Figs. 2, 5, 9, 14.
25.	"designating" / "designated"	'187 patent - claims 1, 3, 5, 7, 9, 11, 12, 14	Plain and ordinary meaning	'187 patent (Exhibit E) at 1:39-43, 1:63-67, 5:40-62, 7:40-48, 9:13-22, 12:18-34; claims 1, 3, 5, 7, 9, 11, 12, 14.	indicating / indicated as a current selection by the controller	'187 patent (Exhibit E) at 5:39-42, 6:9-20, 8:18-30, 8:31-39, 9:53-65, 9:67-10:15, 10:20-25, 11:41-54; Figs. 15, 19; see citations regarding "scheduled," incorporated by reference.
26.	"any available address location"	'187 patent - claims 1, 5, 9, 12	EMC's position is that the proper term to be construed is 'allowing storage device writes to occur … to any available address location of the current write device(s).' That term should be construed to mean: 'Allowing the selection of an address location for a write from the group of all address locations to which data can be	'187 patent (Exhibit E) at 1:31-38, 4:25-44; claims 1, 5, 9, 12. '187 file history excerpts (Exhibit K) at October 28, 2011 Office Action (EMC-PS0002484-2493), February 27, 2012 Request for Continued Examination (EMC-PS0002499, 2506-2507, 2509-2516), March 19, 2012	any unused address location regardless of position	'187 patent (Exhibit E) at 4:31-45; '187 patent file history, Office Action Summary dated October 28, 2011 (Exhibit K) at EMC-PS0002486-EMC-PS0002488; '187 patent file history, Amendment and Response dated February 27, 2012 (Exhibit K) at EMC-PS0002509-EMC-

	CLAIM TERM	PATENT/ CLAIM(S)	EMC'S CONSTRUCTION	EMC'S INTRINSIC EVIDENCE	PURE STORAGE'S CONSTRUCTION	PURE STORAGE'S INTRINSIC EVIDENCE
			written.	Office Action (EMC-PS0002518-2528), June 19, 2012 Request for Reconsideration (EMC-PS0002539-2548), October 22, 2012 Notice of Allowability (EMC-PS0002568-2576).		PS0002515; '187 patent file history, Office Action Summary dated March 19, 2012 (Exhibit K) at EMC-PS0002523-EMC-PS0002524.
27.	"write operations pending" / "pending write operations"	'187 patent - claims 1, 3, 5, 7, 9, 11, 12, 14	Plain and ordinary meaning	'187 patent (Exhibit E) at 2:32-33, 2:44-45, 2:54-55, 5:66-6:6:5, 6:9-20, 8:31-48, 9:50-61, 12:18-34; Figs. 6, 11, 15; claims 1, 3, 5, 7, 9, 11, 12, 14.	write operations in buffer memory queued for the current write device(s)	'187 patent (Exhibit E) at 1:43-47, 4:17-19, 5:66-6:5, 6:20-25, 8:18-23, 12:59-61; Claims 1 and 5; '187 patent file history, Notice of Allowability dated October 22, 2012 (Exhibit K) at EMC-PS0002569-EMC-PS0002575.